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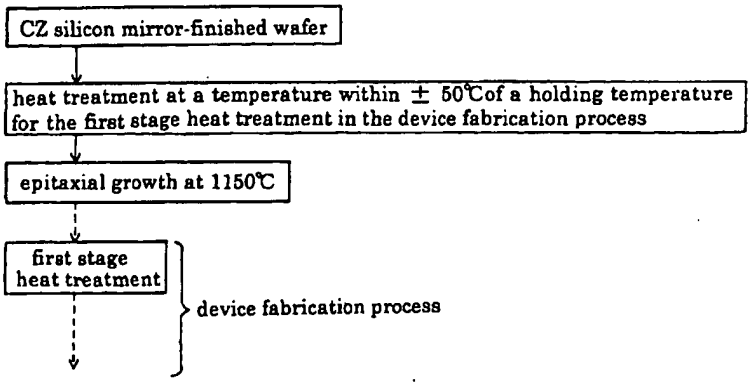
(54) Pre-epitaxial heat treatment method for a silicon epitaxial wafer

(57) Provided is a production method for a silicon epitaxial wafer having an internal gettering capability at a level equal to that of a CZ silicon mirror-finished wafer. In the production method for a silicon epitaxial wafer in which silicon single crystal is epitaxially grown on a silicon wafer; a heat treatment of the silicon wafer is performed at a temperature within ± 50°C of a holding temperature for the first stage heat treatment which is to be firstly effected as a heat treatment in the device fabrication process after the epitaxial growth process for a time period equal to or more than a time period in which a precipitate nucleus from interstitial oxygen in the silicon wafer can grow to a size which survives through the epitaxial growth process, prior to the epitaxial growth process, and thereafter, the epitaxial growth is effected. Preferably the first stage heat treatment is an oxidation process, and the silicon wafer is heated before epitaxy at 700-1000°C for one hour or more. Alternatively the heat treatment is performed during the temperature ramp-up of the epitaxy process itself.

FIG. 1



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Description

BACKGROUND OF THE INVENTION

[0001] This invention relates to a production method for a silicon epitaxial wafer and, more particularly, to a production method for a silicon epitaxial wafer having an internal gettering capability at a level equal to that of a Czochralski (hereinafter abbreviated as CZ) silicon mirror-finished wafer.

[0002] Heretofore, as a semiconductor wafer on which a semiconductor device such as IC, LSI or the like is fabricated, a CZ silicon mirror-finished wafer has generally been used, which is obtained by a procedure in which a wafer is cut from a silicon single crystal which has been grown by being pulled from a silicon melt by means of a CZ method and the wafer is then subjected to mirror polishing on its front surface. The silicon single crystal grown by the CZ method is supersaturated with interstitial oxygen and the interstitial oxygen is precipitated in the form of silicon oxide as the silicon single crystal is cooled down to room temperature after solidification subsequent to a crystal pulling process and due to the precipitation, a number of oxide precipitate nuclei are formed. When an IC or the like is fabricated using a CZ silicon mirror-finished wafer obtained from a silicon single crystal in which a number of the oxide precipitate nuclei are formed, the oxide precipitate nuclei grow to progress oxygen precipitation with the result that a number of microdefects induced by the oxide precipitate nuclei generate in the bulk of the wafer in a heat treatment of the device fabrication process.

[0003] A microdefect induced by an oxide precipitate nucleus preferably works as a gettering site at which heavy metal impurities and the like are captured due to the so-called internal gettering (hereinafter abbreviated as IG) effect when the microdefect exists in the interior region (bulk region). It has known, however, that if microdefects exist in the active region in the vicinity of a wafer surface where semiconductor devices are fabricated, it becomes a factor detrimental to operation of the devices which in turn entails degradation in device characteristics and exerts an adverse influence directly on the device yield.

[0004] In recent years, a demand for a silicon epitaxial wafer has been increased, which is produced by depositing silicon single crystal on a CZ silicon mirror-finished wafer in vapor phase growth (epitaxial growth), as substitution for a CZ silicon mirror-finished wafer, in order to make an active region in the vicinity of a wafer surface where semiconductor devices are fabricated defect free.

[0005] There has, however, been a problem that a silicon epitaxial wafer has a low IG capability compared with a CZ silicon mirror-finished wafer. In other words, in the case of the CZ silicon mirror-finished wafer, since a number of oxide precipitate nuclei are formed in a CZ silicon single crystal while the crystal is cooled down to room temperature after solidification in a crystal pulling process, the oxygen precipitation further progresses in a semiconductor device fabrication process through growth of the precipitate nuclei, whereas, in the case of the silicon epitaxial wafer, since an epitaxial growth process is effected at a temperature as high as the order in the range of 1100 to 1150°C, oxide precipitate nuclei formed in the silicon single crystal pulling process are transited to a solution state during the epitaxial growth process, which suppresses oxygen from precipitation in the semiconductor fabrication process compared with the case of the CZ mirror-finished wafer. Hence, a silicon epitaxial wafer has the IG capability at a low level compared with a CZ silicon mirror-finished wafer.

[0006] In order to solve this problem, external gettering (hereinafter abbreviated as EG) methods have heretofore been employed, in which gettering sites are formed on the rear surface of a silicon epitaxial wafer. For example, as the EG methods, there are named: a sand blast (hereinafter abbreviated as SB) method in which defects are externally formed on the rear surface of a wafer by intention, a PBS method in which a polysilicon film is deposited on the rear surface of a wafer and the like.

[0007] In such conventional methods, a distance between a active region where semiconductor devices are fabricated (on the front surface) and a gettering site (on the rear surface) is long, which problematically causes time for impurities to be captured to be longer. Such circumstances come to be more conspicuous when a semiconductor device fabrication process is performed at a lower temperature, since a time required for an impurity to diffuse up to the rear surface of a wafer is longer. Therefore, an IG method is desirably selected to be in use, in which method a distance between an active region (on the front surface) where semiconductor devices are fabricated and a gettering site (in the bulk) is short.

SUMMARY OF THE INVENTION

[0008] This invention has been made taking such a problem into consideration and it is accordingly an object of the invention to provide a production method for a silicon epitaxial wafer having an IG capability at a level equal to that of a CZ silicon mirror-finished wafer.

[0009] An aspect of the invention there is provided a production method for a silicon epitaxial wafer which is obtained by epitaxially growing silicon single crystal on a silicon wafer and subsequently put into a device fabrication process including a plurality of heat treatments, wherein a heat treatment of the silicon wafer is performed at a temperature within ± 50°C of a holding temperature for the first stage heat treatment which is to be firstly effected as a heat treatment in the device fabrication process after the epitaxial growth process for a time period equal to or mor than a time period in which a

precipitate nucleus from interstitial oxyg n in the silicon wafer can grow to a size a nucleus of which survives through the epitaxial growth process, prior to the epitaxial growth process, and thereafter, the epitaxial growth is effected. Preferably, the first stage heat treatment is a heat treatment for forming an oxide film. The time for the heat treatment prior to the epitaxial growth process is one hour or more. The heat treatment prior to the epitaxial growth process is effected at a temperature in the range of 700 to 1000°C.

[0010] Another aspect of the invention there is provided a production method for a silicon epitaxial wafer which is obtained by epitaxially growing silicon single crystal on a silicon wafer and subsequently put into a device fabrication process including a plurality of heat treatments, wherein a heat treatment of the silicon wafer is performed being kept at a temperature within ± 50°C of a holding temperature for the first stage heat treatment which is to be firstly effected as a heat treatment in the device fabrication process after the epitaxial growth process for a time period equal to or more than a time period in which a precipitate nucleus from interstitial oxygen in the silicon wafer can grow to a size a nucleus of which survives through the epitaxial growth process, in the course of raising temperature after start of the epitaxial growth process, and thereafter, a temperature is raised to an epitaxial growth temperature to perform the epitaxial growth. Preferably, the first stage heat treatment is a heat treatment for forming an oxide film. The time for the heat treatment at a holding temperature in the course of raising temperature after start of the epitaxial growth process is one hour or more. The heat treatment in the course of raising temperature after start of the epitaxial growth process is effected at a holding temperature in the range of 700 to 1000°C.

[0011] In the first aspect of the invention, the silicon wafer is subjected to a heat treatment at a temperature within ± 50°C of a holding temperature for the first stage heat treatment which is to be firstly effected as a heat treatment in the device fabrication process after the epitaxial growth process for a time period equal to or more than a time period in which a precipitate nucleus from interstitial oxygen in the silicon wafer can grow to a size a nucleus of which survives through the epitaxial growth process, prior to the epitaxial growth process. This is to control oxygen precipitation taking advantage of a fact that how much oxide precipitate nuclei in a wafer which have been formed according to the thermal history in the pulling of a single crystal ingot grow to progress oxygen precipitation in the device fabrication process is dependent on the first stage heat treatment temperature in the device fabrication process. That is, a behavior in oxygen precipitation in the first stage heat treatment which is firstly effected as a heat treatment in the semiconductor device fabrication process following the epitaxial growth process is conjectured in advance and an equivalent heat treatment of the first stag heat treatment is effected prior to th epitaxial growth process in advance. By giving a heat treatment on a silicon wafer prior to the epitaxial growth process in this way, oxide precipitate nuclei are remained without assuming a solution state during an epitaxial growth process even when the epitaxial growth is conducted after the heat treatment, so that oxygen precipitation in the semiconductor device fabrication process is not suppressed. Hence, a silicon epitaxial water produced by a method of the invention has an IC capability at a level equal to that of a CZ silicon mirror-finished wafer.

[0012] In the second aspect of the invention, a heat treatment of the silicon wafer is performed being kept at a temperature within ± 50°C of a holding temperature for the first stage heat treatment which is to be firstly effected as a heat treatment in the device fabrication process after the epitaxial growth process for a time period equal to or more than a time period in which a precipitate nucleus from interstitial oxygen in the silicon wafer can grow to a size a nucleus of which survives through the epitaxial growth process, in the course of raising temperature after start of the epitaxial growth process, and thereby, oxide precipitate nuclei are remained without assuming a solution state during an epitaxial growth process even when the epitaxial growth is conducted while temperature is raised up to the epitaxial growth temperature after the heat treatment as described above, so that oxygen precipitation in the semiconductor device fabrication process is not suppressed. Hence, a silicon epitaxial water produced by a method of the invention has an IG capability at a level equal to that of a CZ silicon mirror-finished wafer.

[0013] As the first stage heat treatment which is firstly effected as a heat treatment in the semiconductor device fabrication process, an oxide film forming heat treatment is generally named. The time period in which a precipitate nucleus from interstitial oxygen in a silicon wafer can grow to a size a nucleus of which survives through the epitaxial growth process is preferably one hour or more. In addition, a holding temperature in the heat treatment prior to the epitaxial growth or in the course of raising temperature after start of the epitaxial growth process is preferably in the range of 700 to 1000°C.

[0014] According to the invention, a silicon epitaxial water having an IG capability at a level equal to that of a CZ silicon mirror-finished wafer can be produced. Therefore, even when a CZ silicon mirror-finished wafer used in a device fabrication process is changed to a silicon epitaxial wafer, there arises no anxiety about reduction in the IC capability, which enables the silicon epitaxial wafer to be used at ease.

BRIEF DESCRIPTION OF THE DRAWINGS

[0015]

FIG. 1 is a flow chart showing fabrication steps in an example embodying the invention.

FIG. 2 is a graph showing an example of a heat process.

FIG. 3 is a flow chart showing fabrication steps in a second example embodying the invention.

FIG. 4 is a graph showing a relation of heat treatment temperature and bulk defect d nsity.

DETAILED DESCRIPTION OF THE INVENTION

[0016] Embodiments of the invention will be described with reference to the accompanying drawings. FIG. 1 shows an example embodying the invention. A CZ silicon mirror-finished wafer was subjected to a heat treatment at a temperature within ± 50°C of a holding temperature for the first stage heat treatment in the device fabrication process, for example, for 3 hr and after that, silicon single crystal is deposited in epitaxial growth, for example, at 1150°C to produce a silicon epitaxial wafer. Thereafter, the silicon epitaxial wafer is put into the semiconductor device fabrication process and thereby, semiconductor devices are formed in the vicinity of the surface of the wafer. In the semiconductor device fabrication process, for example, a heat process shown in FIG. 2 is adopted.

[0017] FIG. 3 shows a second example embodying the invention. In order to epitaxially grow silicon single crystal on a CZ silicon mirror-finished wafer, raising temperature of the wafer gets started and the temperature is raised to a temperature within ± 50°C of a holding temperature for the first stage heat treatment in the device fabrication process. The wafer is kept at thus raised temperature, for example, for 3 hr, thereafter, the wafer is further heated up to an epitaxial growth temperature, for example, of 1150°C and silicon single crystal is deposited on the wafer in epitaxial growth to produce a silicon epitaxial wafer. Then, by putting the silicon epitaxial wafer into the semiconductor device fabrication process, semiconductor devices are formed in the vicinity of the surface of the wafer.

Example 1

[0018] A CZ silicon mirror-finished wafer of 16 ppma in the initial interstitial oxygen concentration was subjected to a heat treatment at 850°C for 3 hr and after that, silicon single crystal was deposited in epitaxial growth at 1150°C to a thickness of about 5 μm to produce a silicon epitaxial wafer. Thereafter, the silicon epitaxial wafer was subjected to a heat process which simulates a device fabrication process as shown in FIG. 2 and thereafter, a bulk defect density was measured on the silicon epitaxial wafer by infrared laser scattering tomography. Infrared laser scattering tomography is a method of sensing a defect in which an infrared laser beam is projected into a crystal and the scattering light caused by defects in the crystal is sensed. As a result, the bulk defect density was measured at $1.5 \times 10^9/cm^3$.

Example 2

[0019] A CZ silicon mirror-finished wafer same as that of the example 1 was used and the wafer was heated for epitaxial growth to 850°C and kept at the temperature for 3 hr. Thereafter, a temperature of the wafer was further raised to 1150°C and silicon single crystal was deposited by means of epitaxial growth to a thickness of 5 μm to produce a silicon epitaxial wafer. Then, the silicon epitaxial wafer was subjected to the heat process as shown in FIG. 2 and a bulk defect density was measured by infrared laser scattering tomography. As a result, the bulk defect density was $3 \times 10^9/cm^3$.

Comparative Example 1

[0020] A CZ, silicon mirror-finished wafer same as that of the example 1 was used and the wafer was subjected to the heat process as shown in FIG. 2. Thereafter, a bulk defect density of the wafer was measured by infrared laser scattering tomography. As a result, the bulk defect density was $1.8 \times 10^9/cm^3$.

Comparative example 2

[0021] A CZ silicon mirror-finished wafer same as that of the example 1 was used and silicon single crystal was deposited on the wafer by means of epitaxial growth at 1150°C, without a preheat treatment applied to the wafer, to produce a silicon epitaxial wafer. Thereafter, the wafer was subjected to the heat process shown in FIG. 2 and a bulk defect density was then measured by infrared laser scattering tomography. As a result, the bulk defect density was $4 \times 10^6/cm^3$ (lower limit of detection) or less.

Other Examples and Comparative Examples

[0022] Heat treatments, which correspond to the first stage heat treatment of the heat process, at different temperatures were respectively applied to CZ silicon mirror-finished wafers and thereafter, the wafers were subjected to epitaxial growth to produce silicon epitaxial wafers. In a detailed manner, a plurality of CZ silicon mirror wafers were divided into 7 groups and as the preheat treatments for the epitaxial growth, heat treatments were respectively applied to the groups while different temperatures of heat treatments corresponding to the first stage heat treatment as shown in FIG. 2: 700°C, 750°C, 800°C, 850°C, 900°C, 950°C and 1000°C are assigned to the groups. Heat treatment time periods for the groups were in the range of 1 to 8 hr. Thereafter, the CZ silicon mirror-finished wafers which had respectively received the preheat treatments as described above were subjected to epitaxial growth at 1150°C to the thickness of about 5 μm thereon to produce silicon epitaxial wafers. The 7 groups of silicon epitaxial wafers were respectively subjected to the same heat proc-

esses as the heat process shown in FIG. 2 except the respective first stage heat treatments which were assigned with the temperatures of the preheat treatments. Thus obtained wafers were handled as wafers of the examples embodying the invention. On the other hand, CZ silicon mirror-finished waf rs same as the above described examples which had been subjected to neither the preheat treatments or the epitaxial growth were divided to 7 groups and subjected to the same heat treatments as the heat process shown in FIG. 2 like the examples, wherein the first stage heat treatments were respectively assigned with the corresponding temperatures of the examples. Thus obtained were handled as wafers of the comparative examples. Bulk defect densities were measured on all the wafers from the examples and comparative examples by infrared laser scattering tomography. Results are shown in FIG. 4. The wafers of the examples were found to show bulk defect densities of almost the same order as that of the comparative examples in any individual heat process condition. In other words, it has been confirmed that an IG capability of a CZ silicon mirror-finished wafer is not reduced even after epitaxial growth as far as a temperature of a preheat treatment which is effected prior to the epitaxial growth is set in the range of 700 to 1000°C.

Claims

1. A production method for a silicon epitaxial wafer which is obtained by epitaxially growing silicon single crystal on a silicon wafer and subsequently put into a device fabrication process including a plurality of heat treatments, wherein a heat treatment of the silicon wafer is performed at a temperature within ± 50°C of a holding temperature for the first stage heat treatment which is to be firstly effected as a heat treatment in the device fabrication process after the epitaxial growth process for a time period equal to or more than a time period in which a precipitate nucleus from interstitial oxygen in the silicon wafer can grow to a size a nucleus of which survives through the epitaxial growth process, prior to the epitaxial growth process, and thereafter, the epitaxial growth is effected.

2. A production method for a silicon epitaxial wafer according to claim 1, wherein the first stage heat treatment is a heat treatment for forming an oxide film.

3. A production method for a silicon epitaxial wafer according to claim 1 or 2, wherein the time for the heat treatment prior to the epitaxial growth process is one hour or more.

4. A production method for a silicon epitaxial wafer according to any one of claims 1 to 3, wherein the heat treatment prior to the epitaxial growth process is effected at a temperature in the range of 700 to 1000°C.

5. A production method for a silicon epitaxial wafer which is obtained by epitaxially growing silicon single crystal on a silicon wafer and subsequently put into a device fabrication process including a plurality of heat treatments, wherein a heat treatment of the silicon wafer is performed being kept at a temperature within ± 50°C of a holding temperature for the first stage heat treatment which is to be firstly effected as a heat treatment in the device fabrication process after the epitaxial growth process for a time period equal to or more than a time period in which a precipitate nucleus from interstitial oxygen in the silicon wafer can grow to a size a nucleus of which survives through the epitaxial growth process, in the course of raising temperature after start of the epitaxial growth process, and thereafter, a temperature is raised to an epitaxial growth temperature to perform the epitaxial growth.

6. A production method for a silicon epitaxial wafer according to claim 5, wherein the first stage heat treatment is a heat treatment for forming an oxide film.

7. A production method for a silicon epitaxial wafer according to claim 5 or 6, wherein the time for the heat treatment at a holding temperature in the course of raising temperature after start of the epitaxial growth process is one hour or more.

8. A production method for a silicon epitaxial wafer according to any one of claims 5 to 7, wherein the heat treatment in the course of raising temperature after start of the epitaxial growth process is effected at a holding temperature in the range of 700 to 1000°C.

FIG. 1

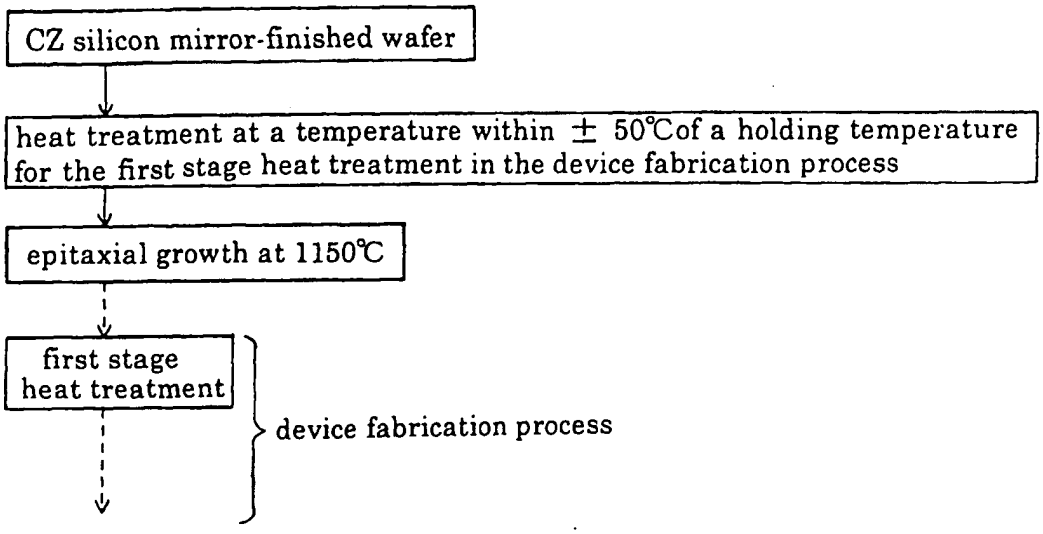
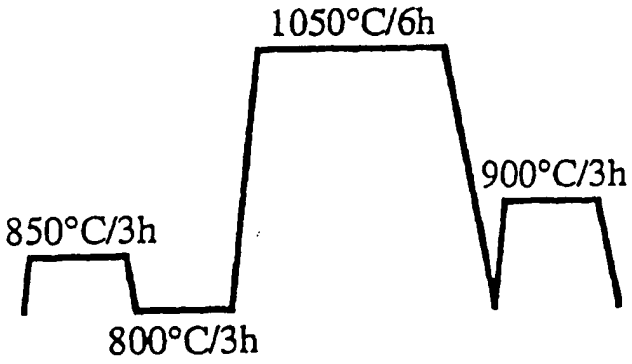

CZ silicon mirror-finished wafer
heat treatment at a temperature within ± 50℃of a holding temperature for the first stage heat treatment in the device fabrication process
epitaxial growth at 1150℃
first stage heat treatment
device fabrication process

FIG. 2


1050°C/6h
900°C/3h
850°C/3h
800°C/3h

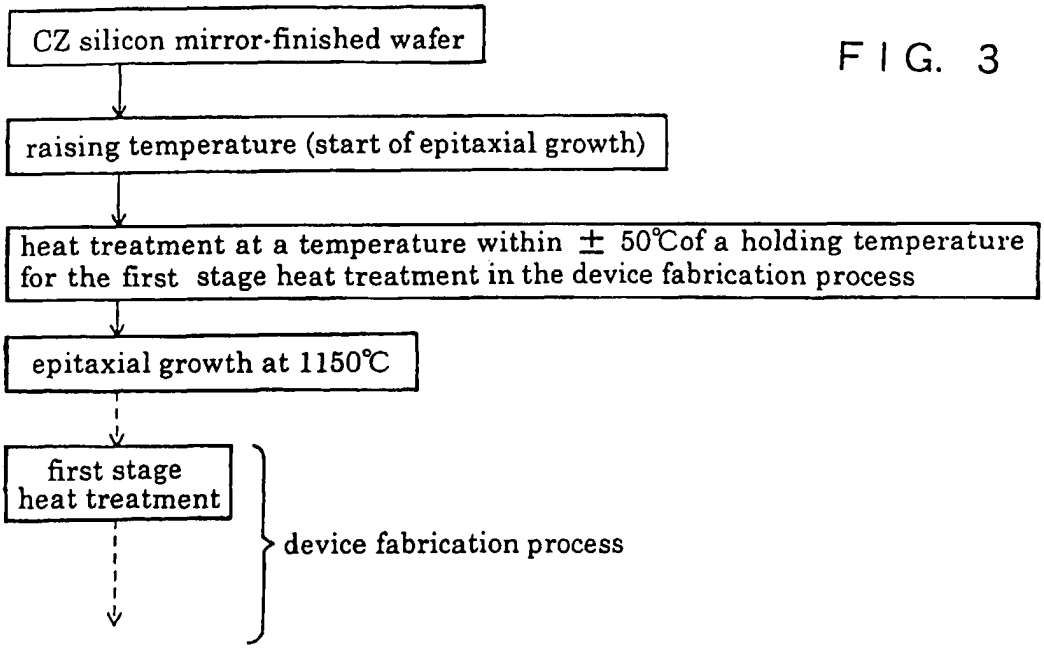

CZ silicon mirror-finished wafer
raising temperature (start of epitaxial growth)
heat treatment at a temperature within ± 50℃of a holding temperature for the first stage heat treatment in the device fabrication process
epitaxial growth at 1150℃
first stage heat treatment
device fabrication process

FIG. 3

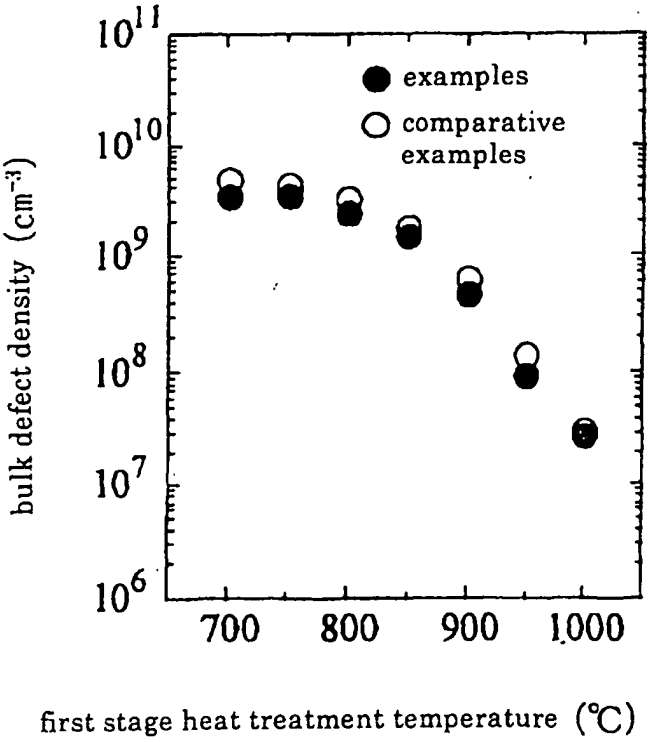

examples
comparative examples
bulk defect density (cm⁻³)
10¹¹
10¹⁰
10⁹
10⁸
10⁷
10⁶
700
800
900
1000
first stage heat treatment temperature (℃)

FIG. 4

European Patent Office

EUROPEAN SEARCH REPORT

Application Number
EP 99 11 0774

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl.6)
X	WIJARANAKULA W ET AL: "INFLUENCE OF THE PREEPITAXIAL ANNEALING AND POLYCRYSTALLINE SILICON DEPOSITION PROCESSES ON OXYGEN PRECIPITATION AND INTERNAL GETTERING IN N/N+(100) EPITAXIAL SILICON WAFERS" JOURNAL OF APPLIED PHYSICS, vol. 65, no. 5, 1 March 1989 (1989-03-01), pages 2078-2083, XP000568094 ISSN: 0021-8979 * the whole document *	1-4	H01L21/20 H01L21/322
X	PATENT ABSTRACTS OF JAPAN vol. 097, no. 001, 31 January 1997 (1997-01-31) & JP 08 250506 A (TOSHIBA CERAMICS CO LTD; TOKUYAMA CERAMICS KK), 27 September 1996 (1996-09-27) * abstract * -& JP 08 250506 A (TOSHIBA CERAMICS CO LTD; TOKUYAMA CERAMICS KK) 27 September 1996 (1996-09-27) * figure 1; table 3 *	5,7,8	
X	PATENT ABSTRACTS OF JAPAN vol. 096, no. 008, 30 August 1996 (1996-08-30) & JP 08 097220 A (TOSHIBA CERAMICS CO LTD; TOKUYAMA CERAMICS KK), 12 April 1996 (1996-04-12) * abstract *	1,3,4	
P,X	WO 98 25299 A (SUMITOMO SITIX CORP; SADAMITSU SHINSUKE ET AL (JP)) 11 June 1998 (1998-06-11) * abstract; figures 1,6 *	1,3,4	

TECHNICAL FIELDS SEARCHED (Int.Cl.6)
H01L
C30B

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
THE HAGUE	17 September 1999	Köpf, C

CATEGORY OF CITED DOCUMENTS

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17-09-1999

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
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JP 08097220 A	12-04-1996	NONE	
WO 9825299 A	11-06-1998	JP 10223641 A	21-08-1998

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